N-Channel 550 V (D-S) Power MOSFET

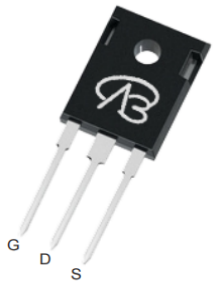
PRODUCT SUMMARY		
V_{DS} (V)	550	
$R_{DS(on)}$ (Ω)	V_{GS} = 10 V	0.250
Q_g (Max.) (nC)	310	
Q_{gs} (nC)	80	
Q_{gd} (nC)	150	
Configuration	Single	

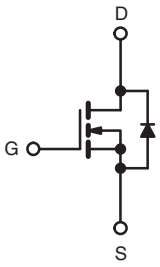
FEATURES

- Low Gate Charge Q_g Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Low $R_{DS(on)}$
- Compliant to RoHS Directive 2002/95/EC

Pb Available

TO-247





N-Channel MOSFET

APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)					
PARAMETER			**SYMBOL**	**LIMIT**	**UNIT**
Drain-Source Voltage			V_{DS}	550	V
Gate-Source Voltage			V_{GS}	± 20	
Continuous Drain Current	V_{GS} at 10 V	T_C = 25 °C	I_D	20	A
		T_C = 100 °C		12	
Pulsed Drain Current[a]			I_{DM}	60	
Linear Derating Factor				4.3	W/°C
Single Pulse Avalanche Energy[b]			E_{AS}	850	mJ
Repetitive Avalanche Current[a]			I_{AR}	50	A
Repetitive Avalanche Energy[a]			E_{AR}	51	mJ
Maximum Power Dissipation	T_C = 25 °C		P_D	530	W
Peak Diode Recovery dV/dt[c]			dV/dt	9.0	V/ns
Operating Junction and Storage Temperature Range			T_J, T_{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s			300[d]	

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Starting T_J = 25 °C, L = 0.82 mH, R_g = 25 Ω, I_{AS} = 47 A (see fig. 12c).
c. I_{SD} ≤ 47 A, dI/dt ≤ 230 A/μs, V_{DD} ≤ V_{DS}, T_J ≤ 150 °C.
d. 1.6 mm from case.

THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum Junction-to-Ambient	R_{thJA}	-	40	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.24	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.23	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static							
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA		550	-	-	A
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA		-	0.60	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		3.0	-	5.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 30 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 440 V, V_{GS} = 0 V		-	-	50	µA
		V_{DS} = 440 V, V_{GS} = 0 V, T_J = 125 °C		-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 28 A[b]	-	0.250	-	Ω
Forward Transconductance	g_{fs}	V_{DS} = 50 V, I_D = 28 A		23	-	-	S
Dynamic							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	2400	-	pF
Output Capacitance	C_{oss}			-	960	-	
Reverse Transfer Capacitance	C_{rss}			-	120	-	
Output Capacitance	C_{oss}	V_{GS} = 0 V	V_{DS} = 1.0 V, f = 1.0 MHz	-	270	-	
			V_{DS} = 400 V, f = 1.0 MHz	-	240	-	
Effective Output Capacitance	C_{oss} eff.		V_{DS} = 0 V to 400 V[c]	-	440	-	
Total Gate Charge	Q_g	V_{GS} = 10 V	I_D = 47 A, V_{DS} = 400 V, see fig. 6 and 13[b]	-	-	350	nC
Gate-Source Charge	Q_{gs}			-	-	85	
Gate-Drain Charge	Q_{gd}			-	-	180	
Turn-On Delay Time	$t_{d(on)}$		V_{DD} = 250 V, I_D = 47 A, R_G = 1.0 Ω, see fig. 10[b]	-	25	-	ns
Rise Time	t_r			-	140	-	
Turn-Off Delay Time	$t_{d(off)}$			-	55	-	
Fall Time	t_f			-	74	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	20	A
Pulsed Diode Forward Current[a]	I_{SM}			-	-	60	
Body Diode Voltage	V_{SD}	T_J = 25 °C, I_S = 47 A, V_{GS} = 0 V[b]		-	-	1.5	V
Body Diode Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = 47 A, dI/dt = 100 A/µs[b]		-	60	120	ns
Body Diode Reverse Recovery Charge	Q_{rr}			-	14	21	µC
Body Diode Recovery Current	I_{RRM}			-	38	-	A
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width ≤ 400 µs; duty cycle ≤ 2 %.
c. C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS}.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

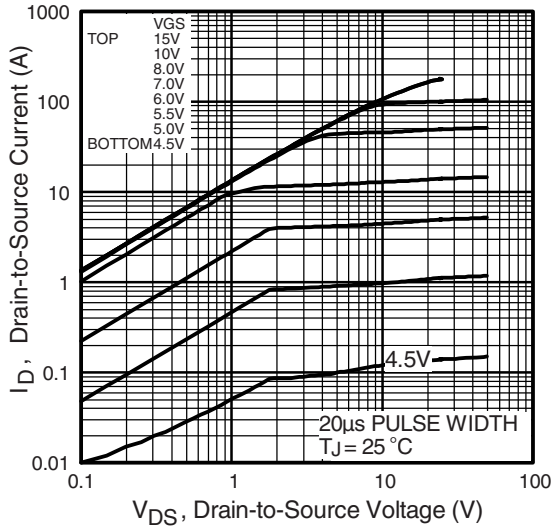


Fig. 1 - Typical Output Characteristics

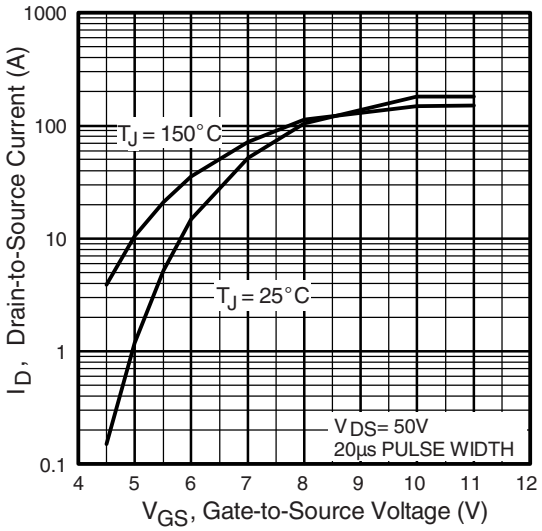


Fig. 3 - Typical Transfer Characteristics

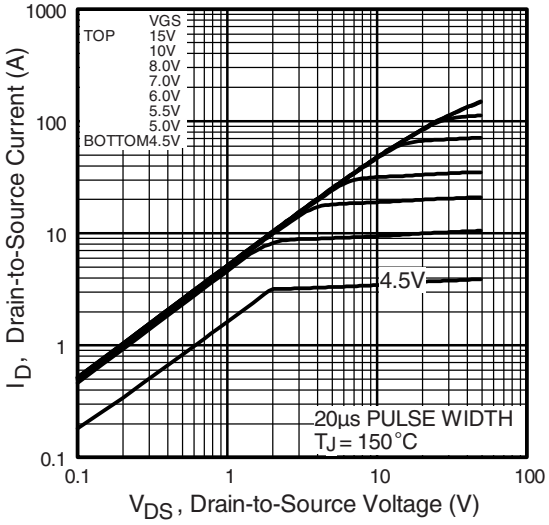


Fig. 2 - Typical Output Characteristics

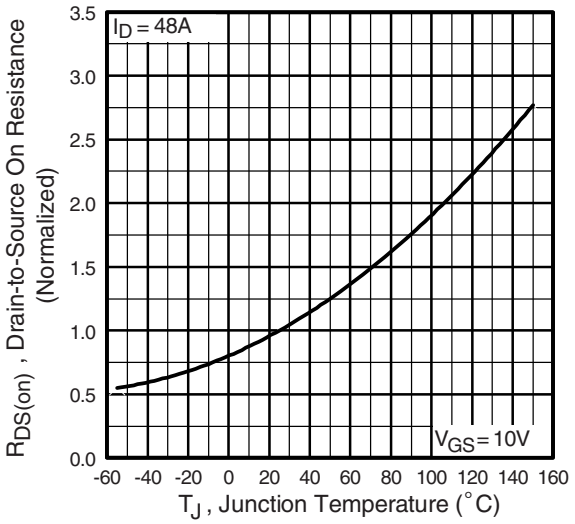


Fig. 4 - Normalized On-Resistance vs. Temperature

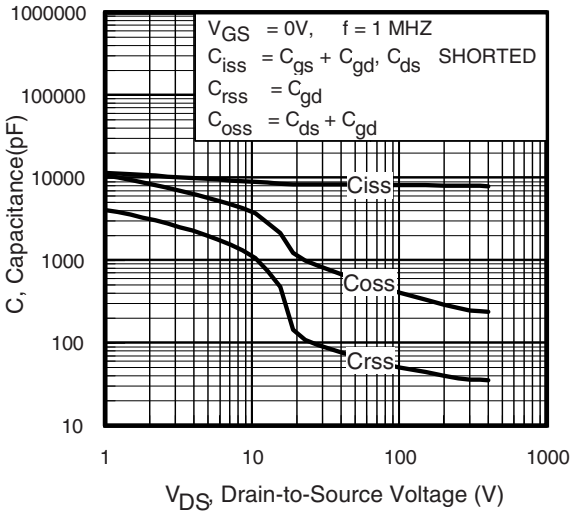


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

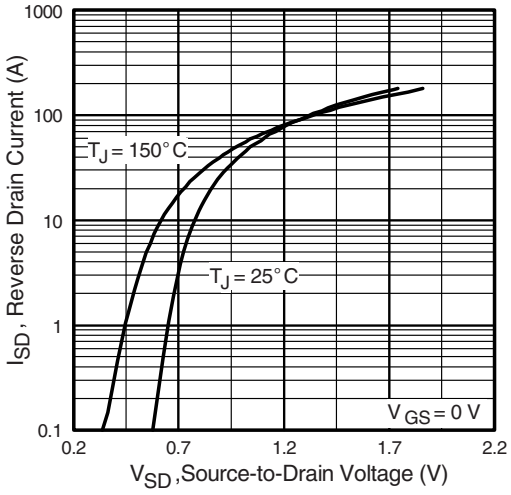


Fig. 7 - Typical Source-Drain Diode Forward Voltage

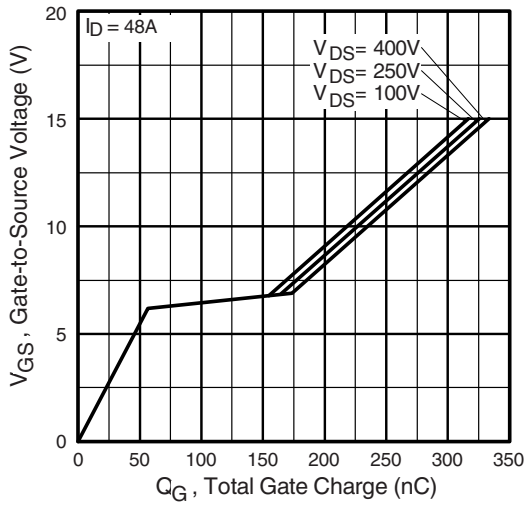


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

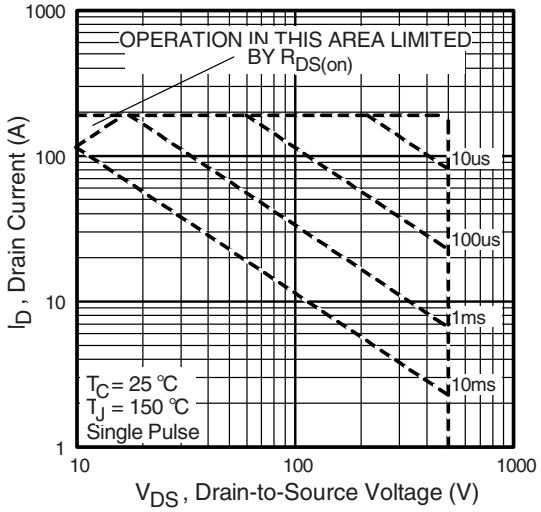


Fig. 8 - Maximum Safe Operating Area

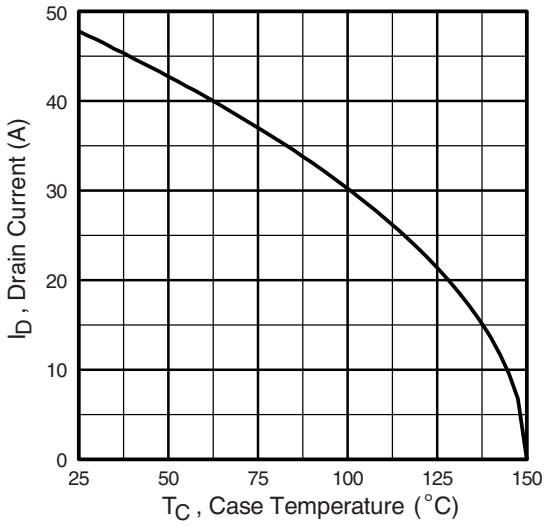


Fig. 9 - Maximum Drain Current vs. Case Temperature

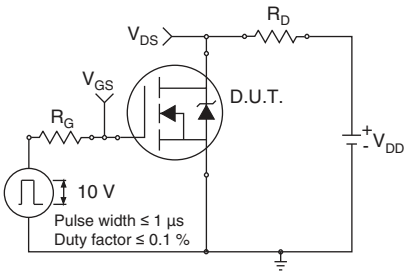


Fig. 10a - Switching Time Test Circuit

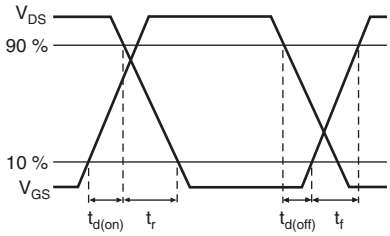


Fig. 10b - Switching Time Waveforms

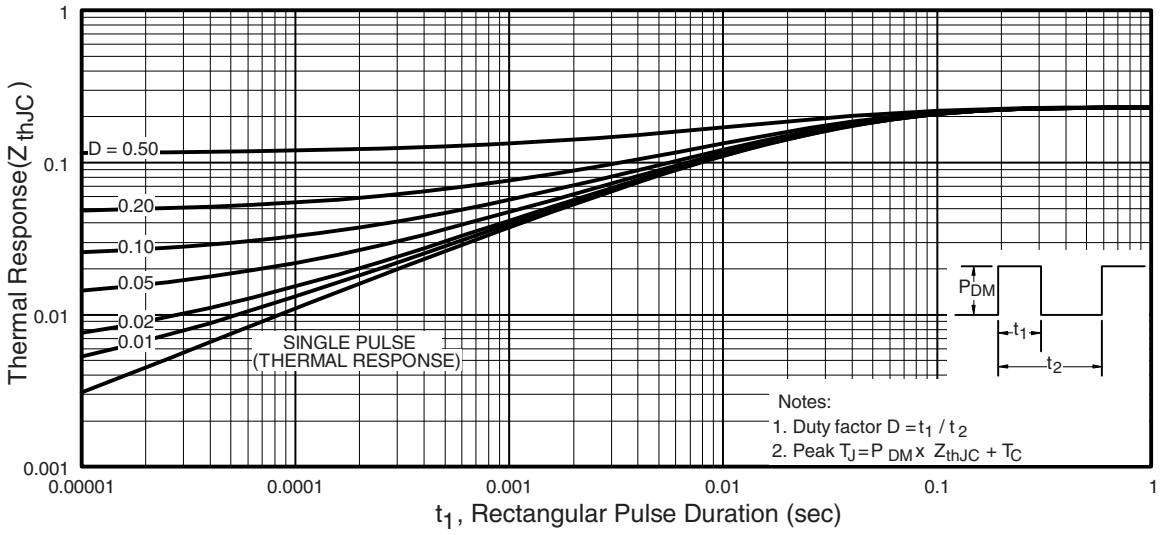


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

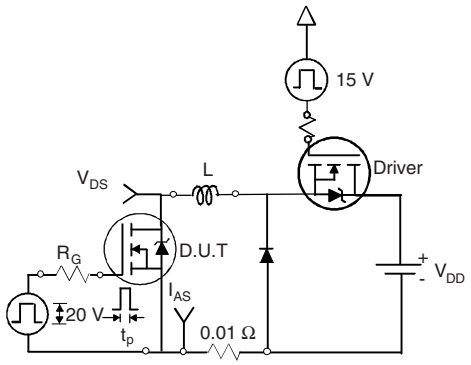


Fig. 12a - Unclamped Inductive Test Circuit

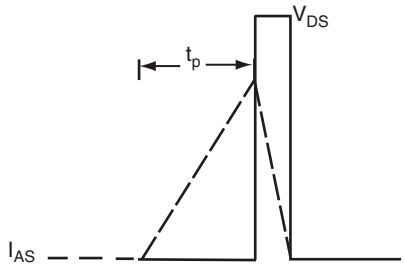


Fig. 12b - Unclamped Inductive Waveforms

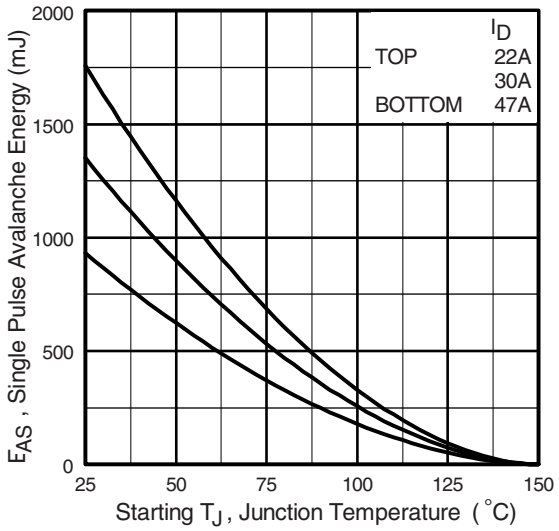


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

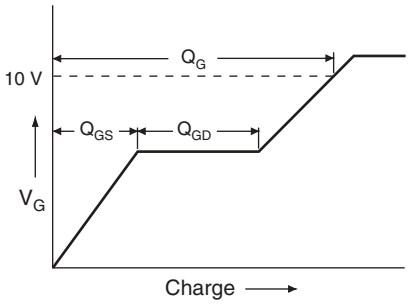


Fig. 13a - Basic Gate Charge Waveform

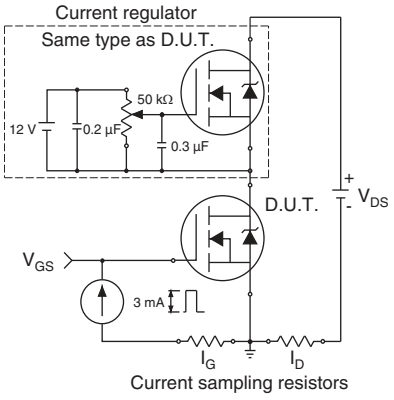
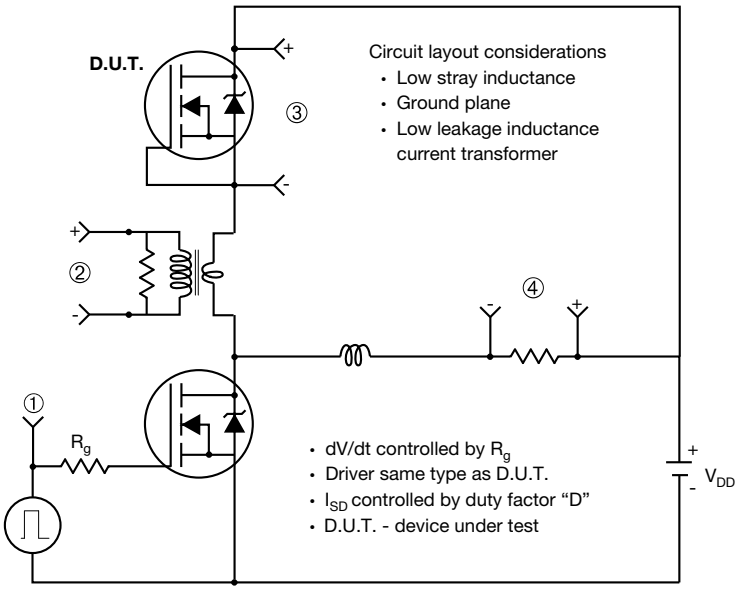
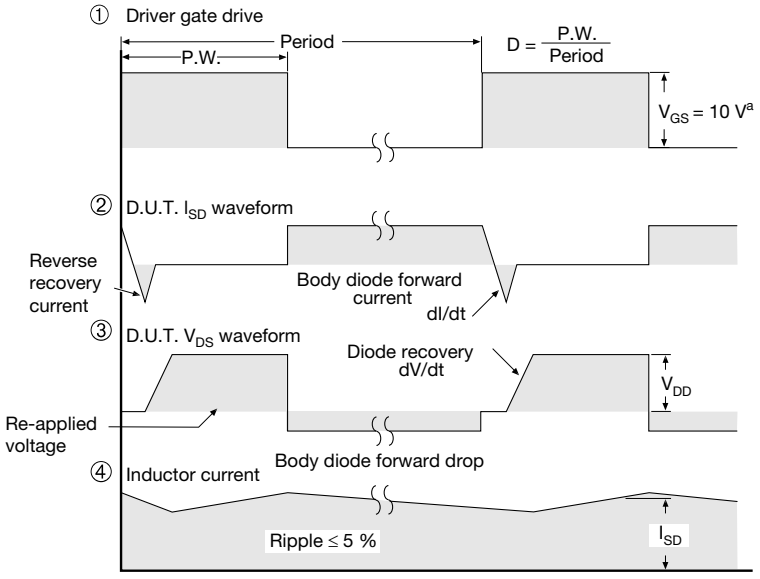


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



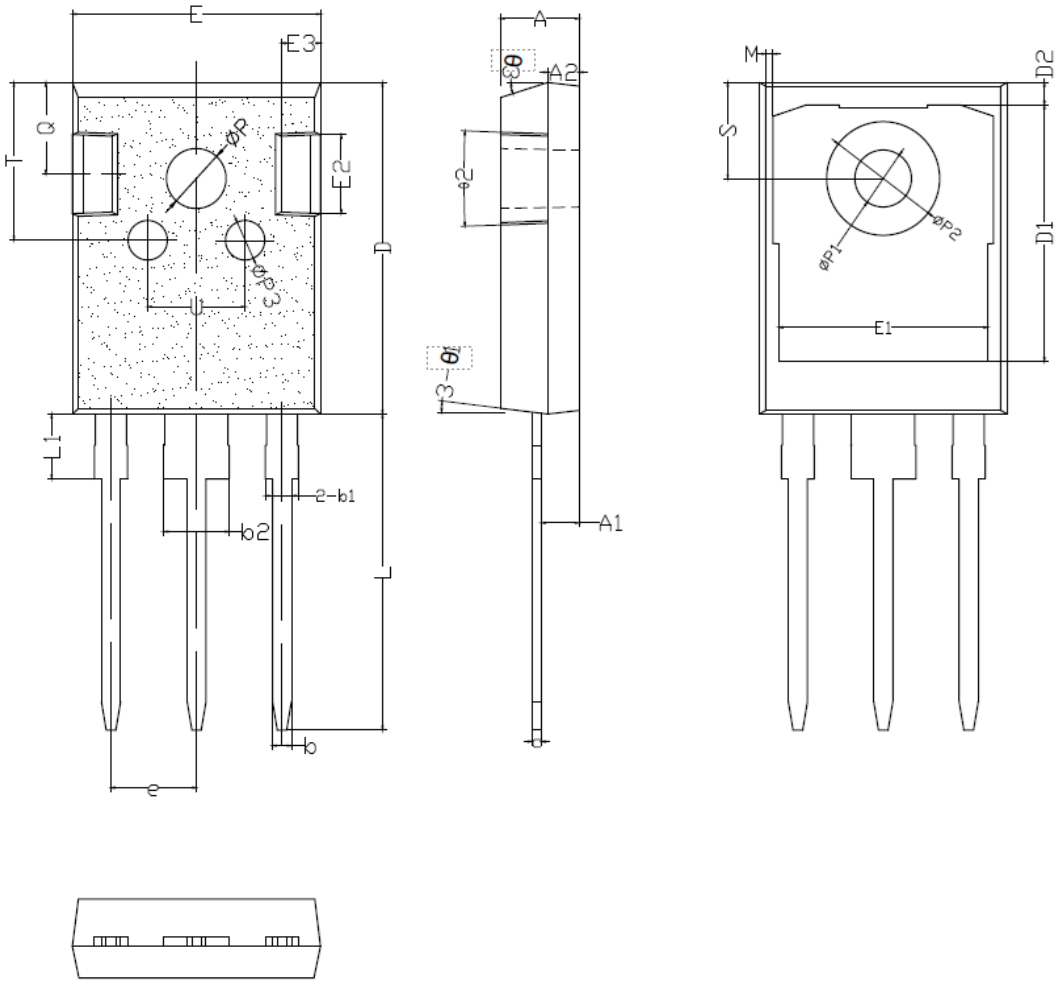


Note

a. V_{GS} = 5 V for logic level devices

Fig. 14 - For N-Channel

TO-247 PACKAGE OUTLINE DIMENSIONS



SYMBOL	mm		
	MIN	NOM	MAX
*A	4.90	5.00	5.10
*A1	2.31	2.41	2.51
A2	1.90	2.00	2.10
*b	1.15	1.20	1.25
*b1	1.95	2.10	2.25
*b2	2.95	3.10	3.25
*c	0.55	0.60	0.65
*D	20.90	21.00	21.10
D1	16.35	16.55	16.75
D2	1.05	1.20	1.35

*E	15.70	15.80	15.90
E1	13.10	13.25	13.40
E2	4.85	4.95	5.10
E3	2.40	2.50	2.60
*e	5.40	5.44	5.48
*L	19.80	19.98	20.15
*L1	-	-	4.30
*ΦP	3.40	3.50	3.60
*ΦP1	6.90	7.10	7.30
ΦP2	2.40	2.50	2.60
ΦP3	2.40	2.50	2.60
Q	5.60	5.80	6.00
*S	6.05	6.15	6.25
T	9.80	10.00	10.20
U	6.00	6.20	6.40
θ1	5°	7°	9°
θ2	1°	3°	5°
θ3	13°	15°	17°

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