Complementary 20 V (D-S) MOSFET

PRODUCT SUMMARY			
	V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
N-Channel	20	0.032 at V_{GS} = 4.5 V	5.9
		0.036 at V_{GS} = 2.5 V	5.6
		0.042 at V_{GS} = 1.8 V	5.2
P-Channel	- 20	0.069 at V_{GS} = - 4.5 V	- 4.1
		0.097 at V_{GS} = - 2.5 V	- 3.4
		0.137 at V_{GS} = - 1.8 V	- 2.9

FEATURES

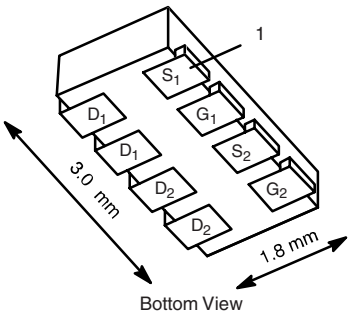
- **Halogen-free According to IEC 61249-2-21 Definition**
- Trench Power MOSFETs
- Ultra Low $R_{DS(on)}$ and Excellent Power Handling In Compact Footprint
- Compliant to RoHS Directive 2002/95/EC

Pb-free
RoHS COMPLIANT
HALOGEN FREE Available

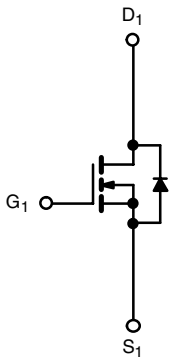
APPLICATIONS

- Load Switching for Portable Devices

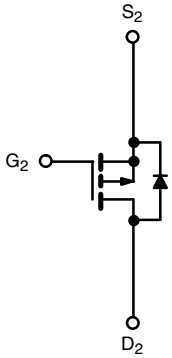
DFN 3x2



Bottom View



N-Channel MOSFET



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted								
			N-Channel		P-Channel		
Parameter		Symbol	5 s	Steady State	5 s	Steady State	Unit
Drain-Source Voltage		V_{DS}	20		- 20		V
Gate-Source Voltage		V_{GS}	± 8				
Continuous Drain Current (T_J = 150 °C)[a]	T_A = 25 °C	I_D	5.9	4.4	- 4.1	- 3	A
	T_A = 85 °C		4.2	3.1	- 2.9	- 2.2	
Pulsed Drain Current		I_{DM}	20		- 15		
Continuous Source Current (Diode Conduction)[a]		I_S	1.8	0.9	- 1.8	- 0.9	
Maximum Power Dissipation[a]	T_A = 25 °C	P_D	2.1	1.1	2.1	1.1	W
	T_A = 85 °C		1.1	0.6	1.1	0.6	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150				°C
Soldering Recommendations (Peak Temperature)[b, c]			260				

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a]	t ≤ 5 s	R_{thJA}	50	60	°C/W
	Steady State		90	110	
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	30	40	

Notes:

a. Surface mounted on 1" x 1" FR4 board.

b. See Reliability Manual for profile. The DFN3X2 is a leadless package. The end of t he lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

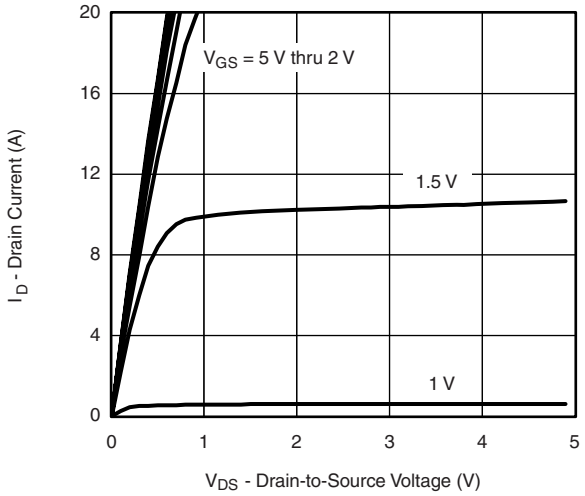
c. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

SPECIFICATIONS T_J = 25 °C, unless otherwise noted							
Parameter	**Symbol**	**Test Conditions**		**Min.**	**Typ.**	**Max.**	**Unit**
Static							
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	N-Ch	0.4		1.0	V
		V_{DS} = V_{GS}, I_D = - 250 µA	P-Ch	- 0.4		- 1.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 8 V	N-Ch			± 100	nA
			P-Ch			± 100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V	N-Ch			1	µA
		V_{DS} = - 20 V, V_{GS} = 0 V	P-Ch			- 1	
		V_{DS} = 20 V, V_{GS} = 0 V, T_J = 85 °C	N-Ch			5	
		V_{DS} = - 20 V, V_{GS} = 0 V, T_J = 85 °C	P-Ch			- 5	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 4.5 V	N-Ch	20			A
		V_{DS} ≤ - 5 V, V_{GS} = - 4.5 V	P-Ch	- 15			
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = 4.5 V, I_D = 4.4 A	N-Ch		0.032		Ω
		V_{GS} = - 4.5 V, I_D = - 3 A	P-Ch		0.069		
		V_{GS} = 2.5 V, I_D = 4.1 A	N-Ch		0.036		
		V_{GS} = - 2.5 V, I_D = - 2.5 A	P-Ch		0.097		
		V_{GS} = 1.8 V, I_D = 1.9 A	N-Ch		0.042		
		V_{GS} = - 1.8 V, I_D = - 0.6 A	P-Ch		0.137		
Forward Transconductance[a]	g_{fs}	V_{DS} = 10 V, I_D = 4.4 A	N-Ch		22		S
		V_{DS} = - 10 V, I_D = - 3 A	P-Ch		8		
Diode Forward Voltage[a]	V_{SD}	I_S = 0.9 A, V_{GS} = 0 V	N-Ch		0.8	1.2	V
		I_S = - 0.9 A, V_{GS} = 0 V	P-Ch		- 0.8	- 1.2	
Dynamic[b]							
Total Gate Charge	Q_g	N-Channel V_{DS} = 10 V, V_{GS} = 4.5 V, I_D = 4.4 A P-Channel V_{DS} = - 10 V, V_{GS} = - 4.5 V, I_D = - 3 A	N-Ch		5	7.5	nC
			P-Ch		5.5	8.5	
Gate-Source Charge	Q_{gs}		N-Ch		0.85		
			P-Ch		0.91		
Gate-Drain Charge	Q_{gd}		N-Ch		1		
			P-Ch		1.6		
Turn-On Delay Time	$t_{d(on)}$	N-Channel V_{DD} = 10 V, R_L = 10 Ω I_D ≅ 1 A, V_{GEN} = 4.5 V, R_g = 6 Ω P-Channel V_{DD} = - 10 V, R_L = 10 Ω I_D ≅ - 1 A, V_{GEN} = - 4.5 V, R_g = 6 Ω	N-Ch		20	30	ns
			P-Ch		18	30	
Rise Time	t_r		N-Ch		36	55	
			P-Ch		32	50	
Turn-Off Delay Time	$t_{d(off)}$		N-Ch		30	45	
			P-Ch		42	65	
Fall Time	t_f		N-Ch		12	20	
			P-Ch		26	40	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 0.9 A, dI/dt = 100 A/µs	N-Ch		45	90	
		I_F = - 0.9 A, dI/dt = 100 A/µs	P-Ch		30	60	

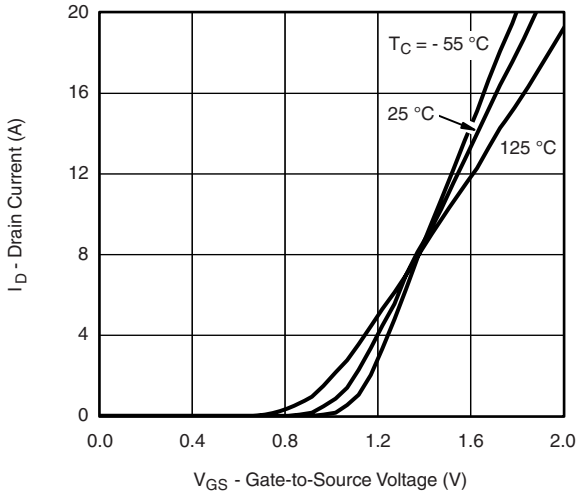
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

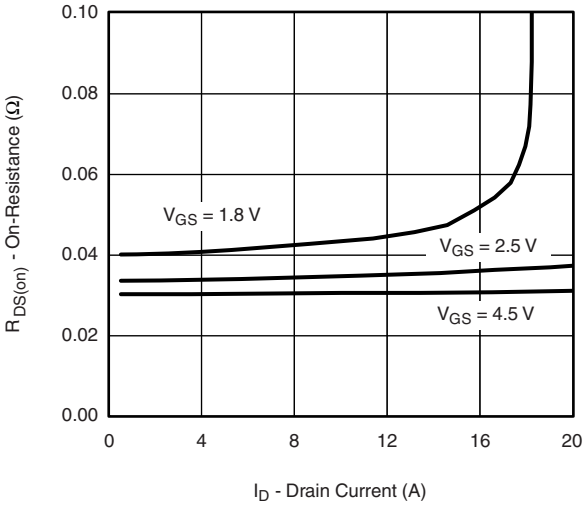
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



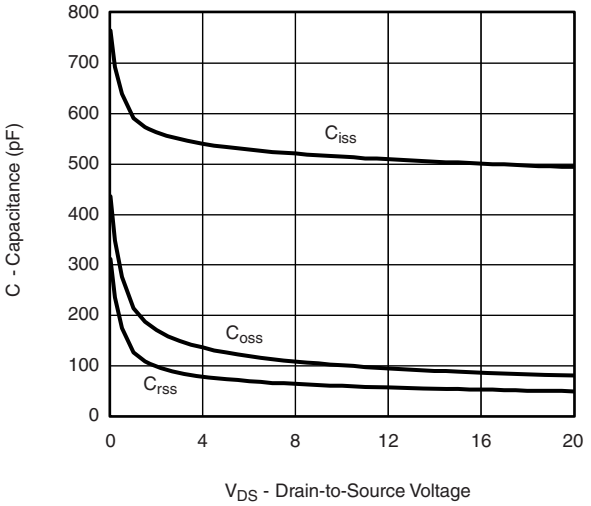
Output Characteristics



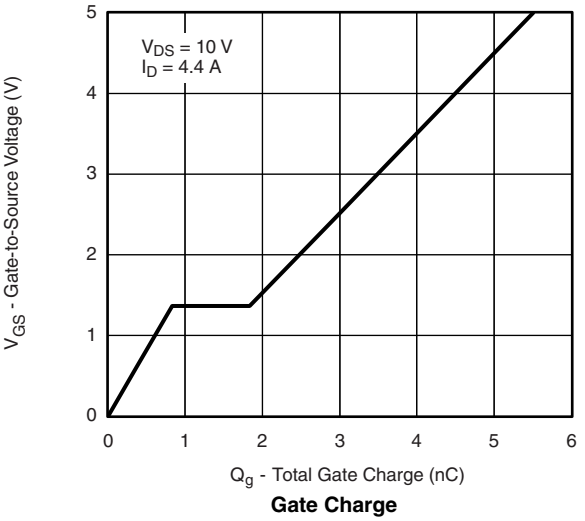
Transfer Characteristics



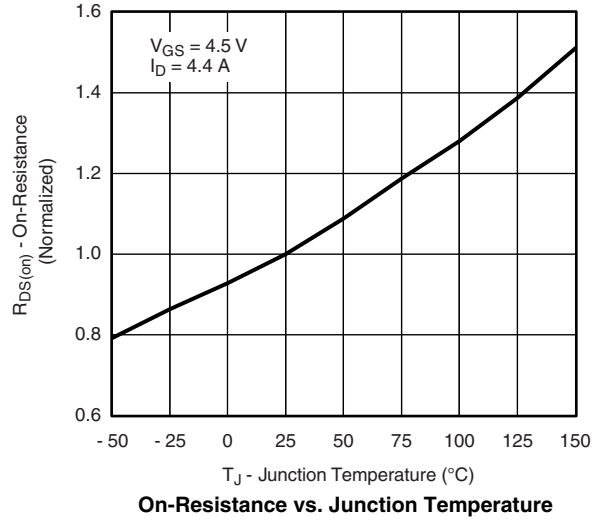
On-Resistance vs. Drain Current



Capacitance

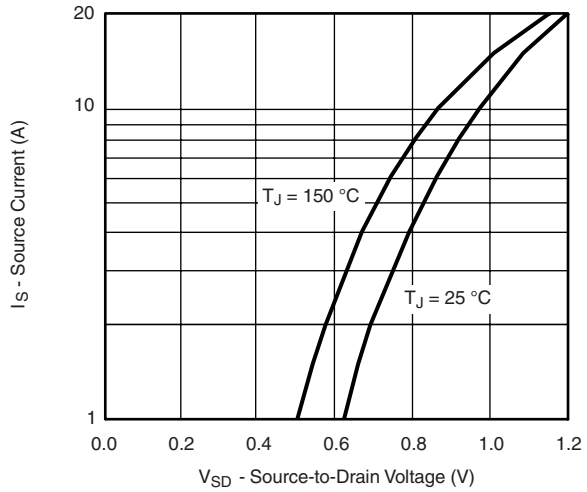


Gate Charge

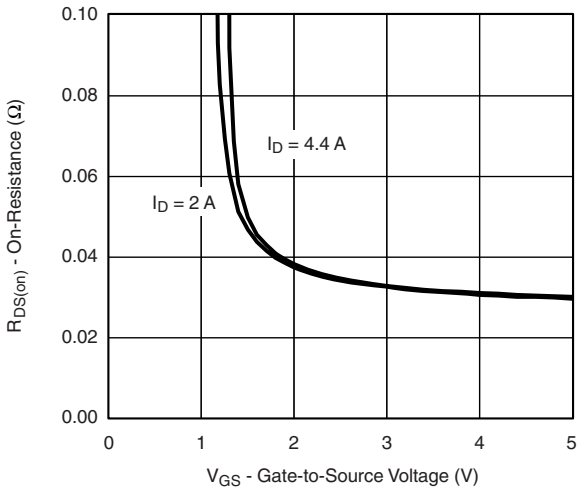


On-Resistance vs. Junction Temperature

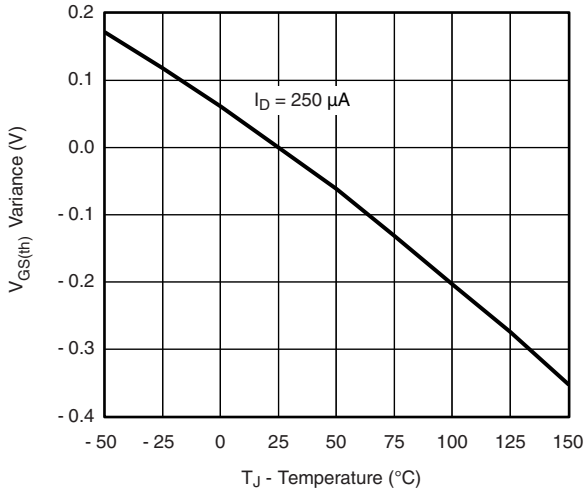
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



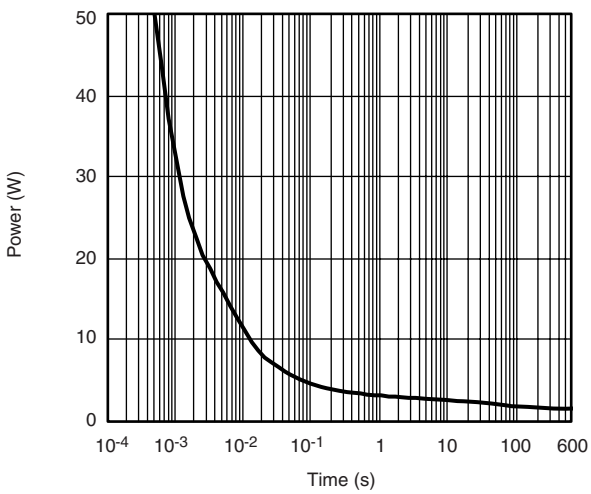
Source-Drain Diode Forward Voltage



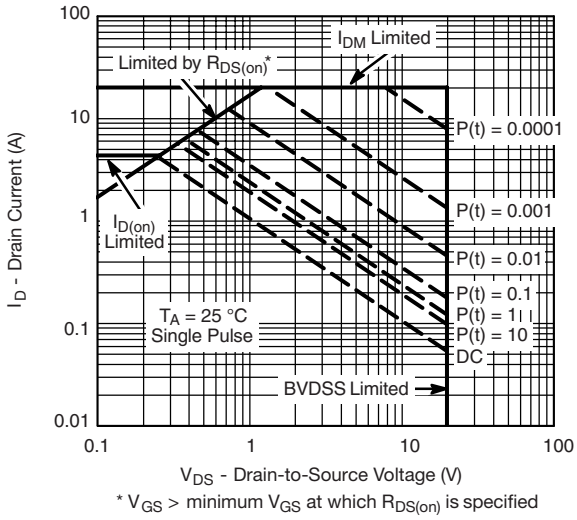
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



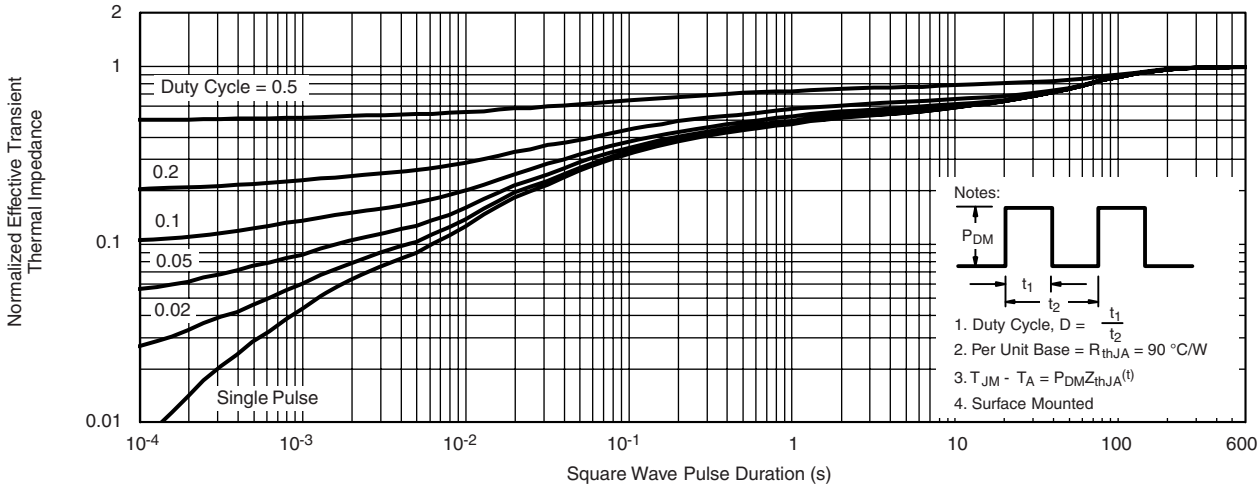
Single Pulse Power



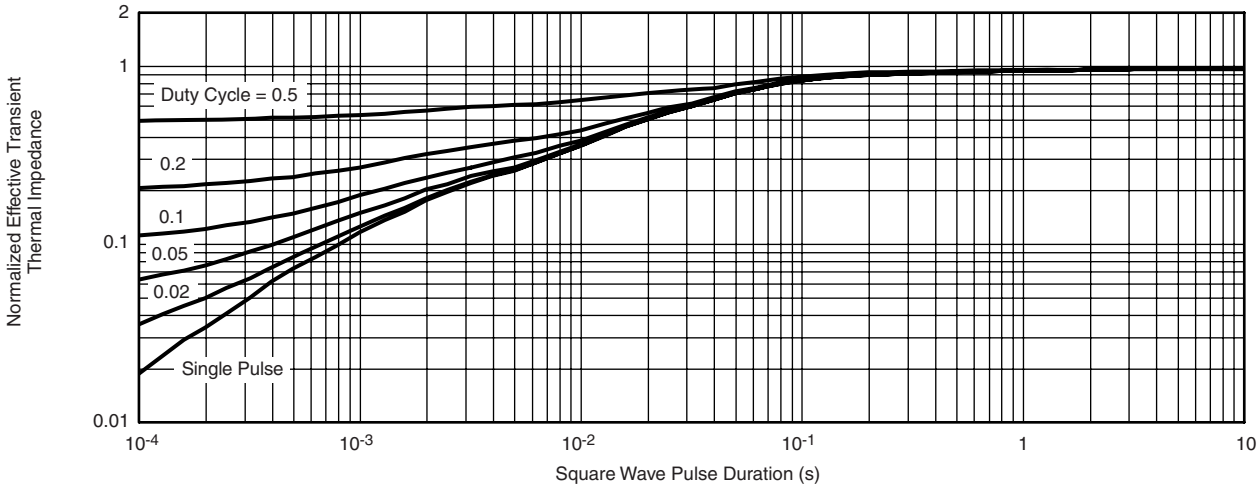
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area

N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

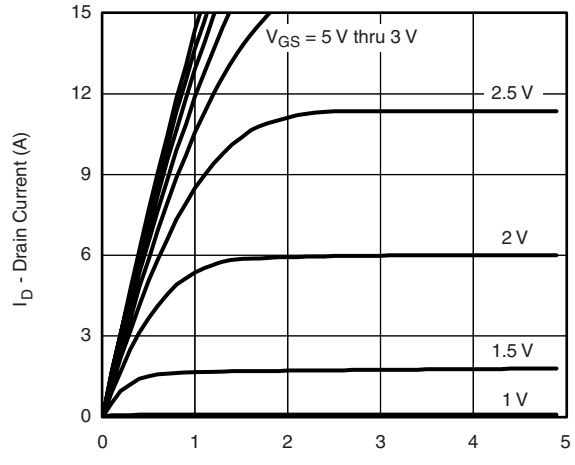


Normalized Thermal Transient Impedance, Junction-to-Ambient

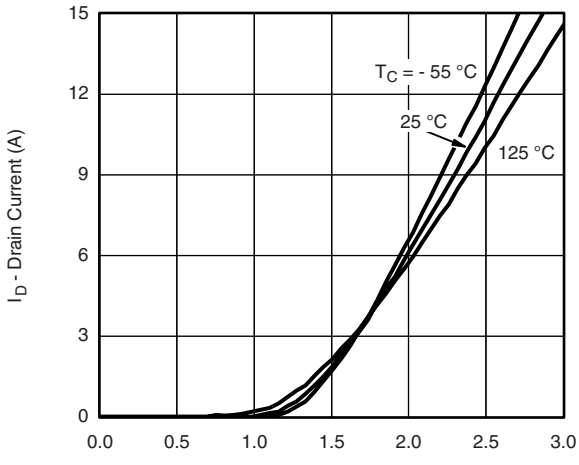


Normalized Thermal Transient Impedance, Junction-to-Foot

P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

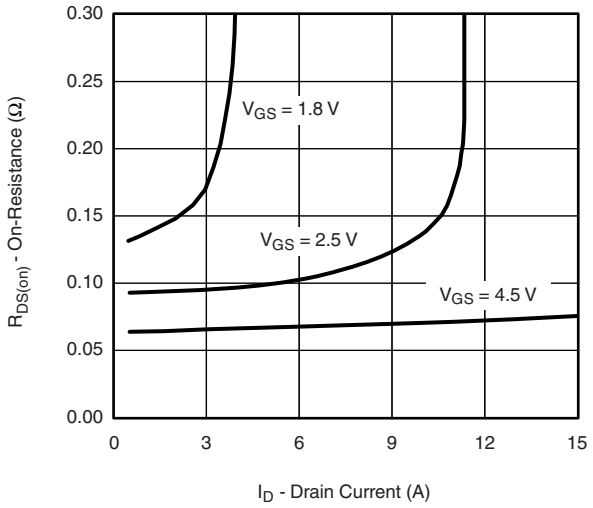


Output Characteristics

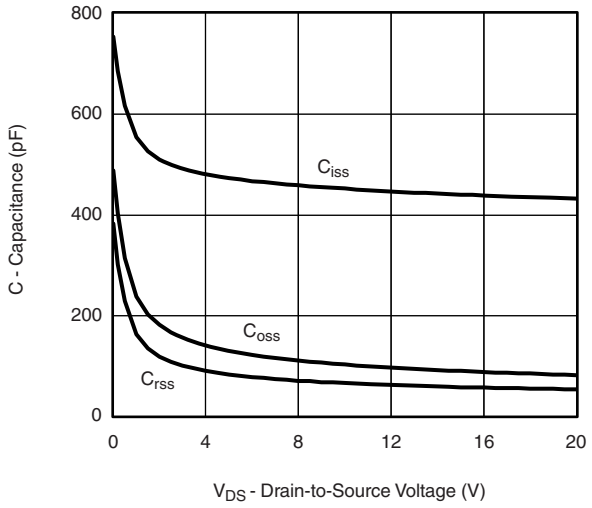


Transfer Characteristics

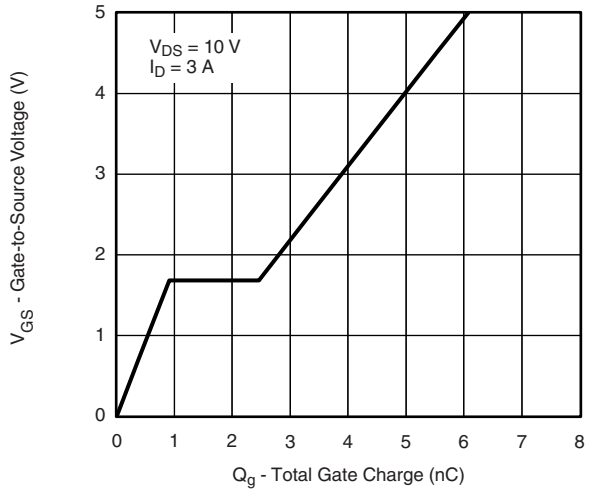
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



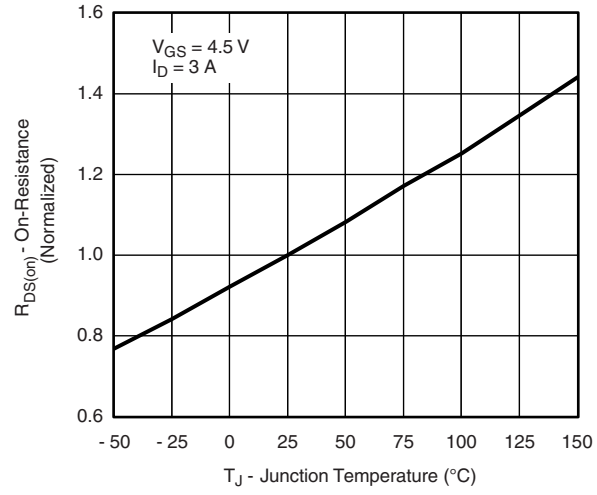
On-Resistance vs. Drain Current



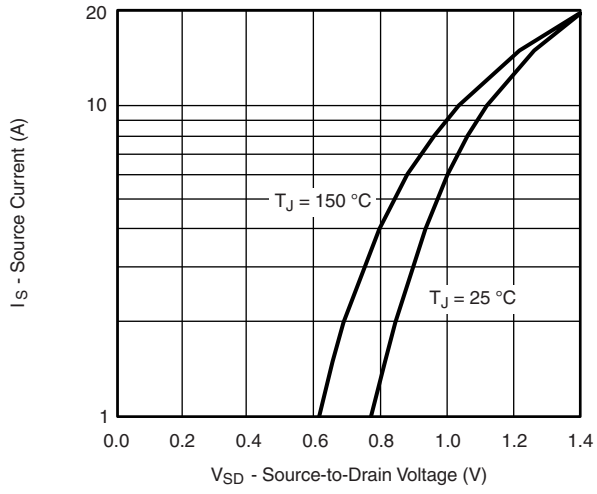
Capacitance



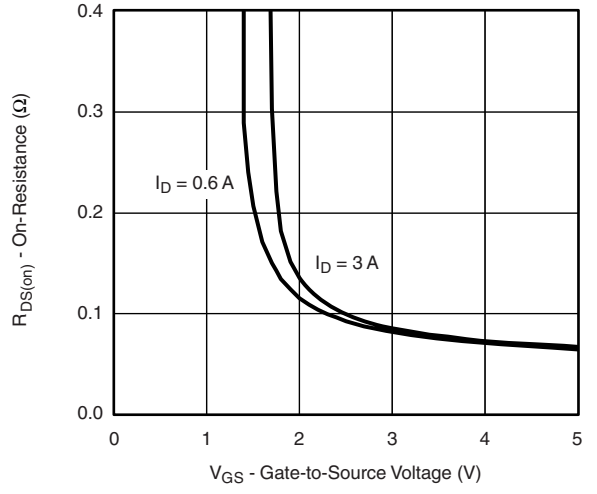
Gate Charge



On-Resistance vs. Junction Temperature

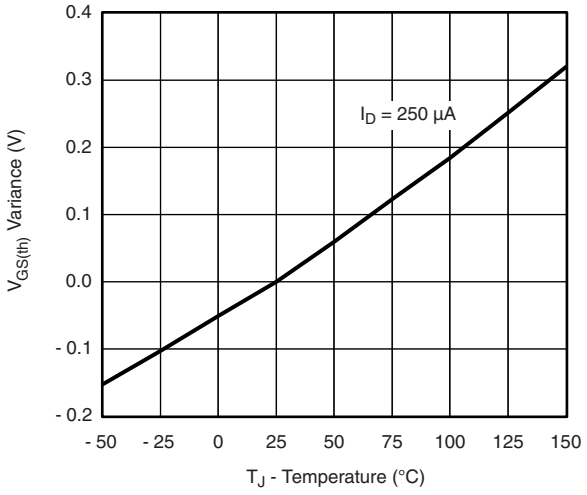


Source-Drain Diode Forward Voltage

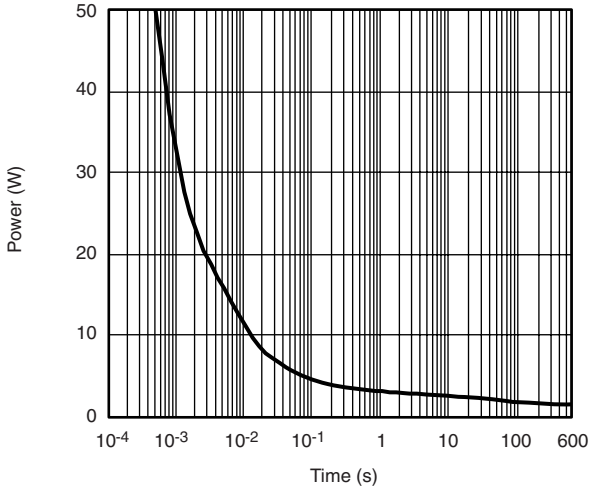


On-Resistance vs. Gate-to-Source Voltage

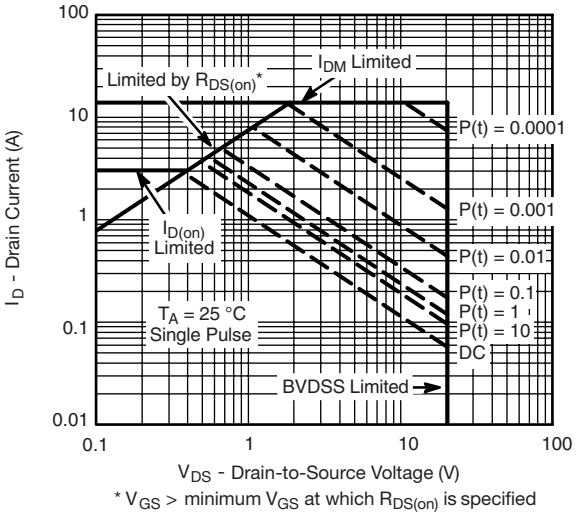
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Threshold Voltage

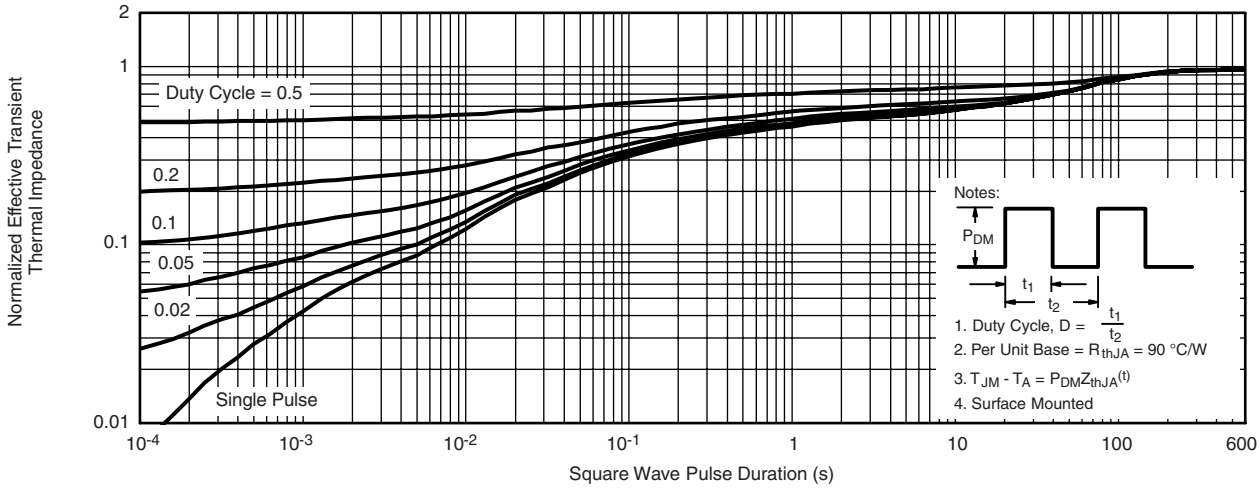


Single Pulse Power



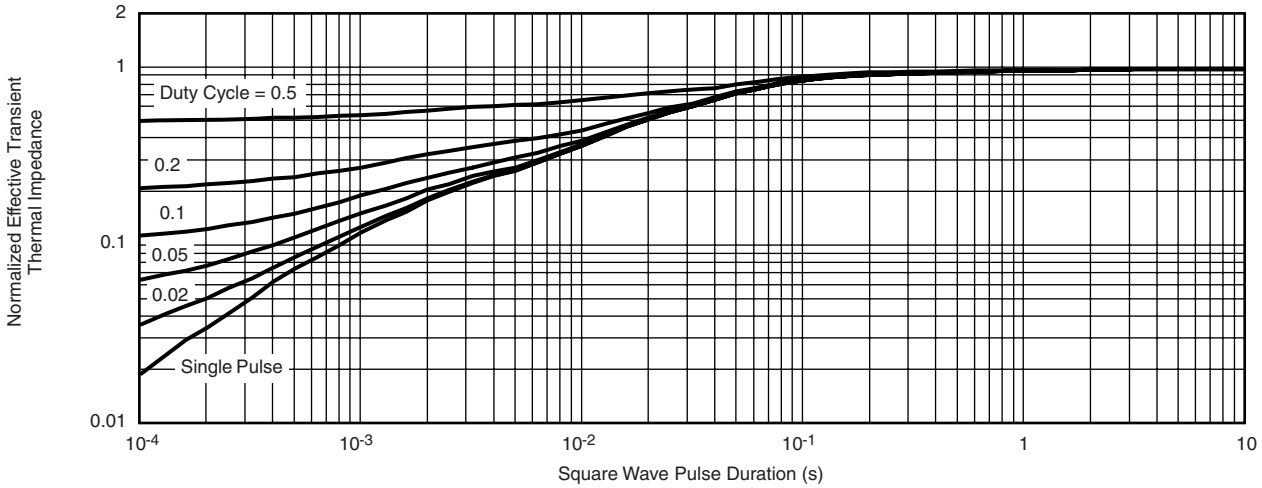
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area



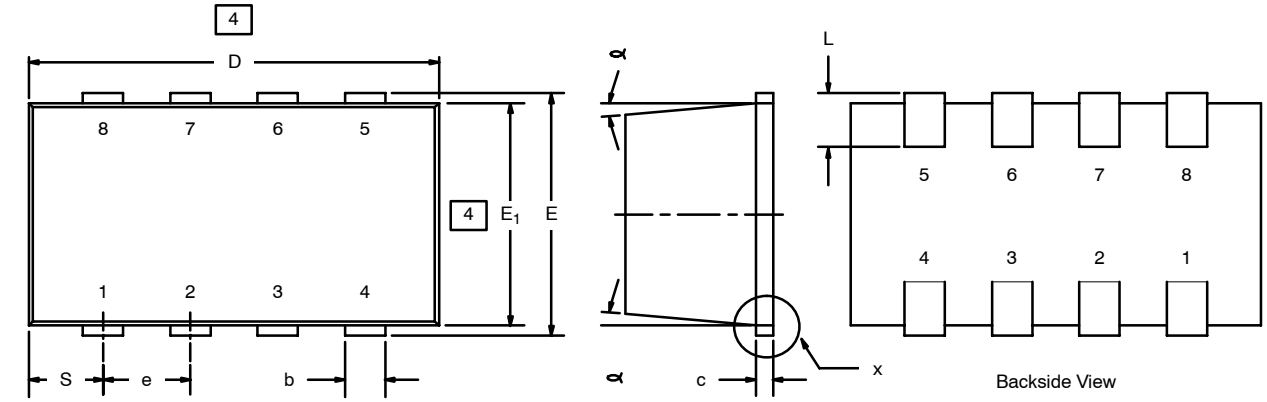
Normalized Thermal Transient Impedance, Junction-to-Ambient

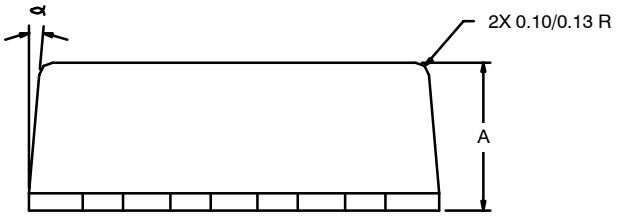
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

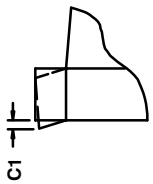


Normalized Thermal Transient Impedance, Junction-to-Foot

DFN 3x2







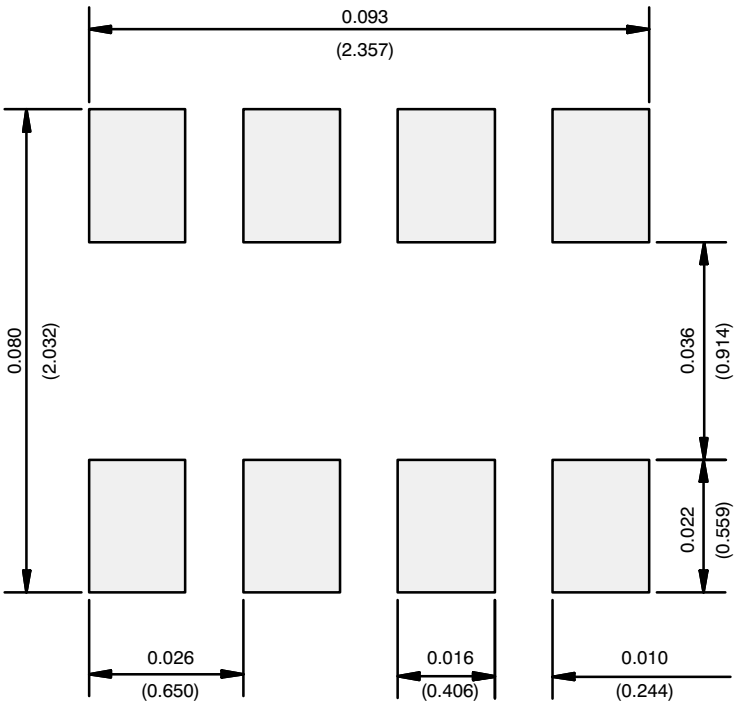
DETAIL X

NOTES:

1. All dimensions are in millimeaters.
2. Mold gate burrs shall not exceed 0.13 mm per side.
3. Leadframe to molded body offset is horizontal and vertical shall not exceed 0.08 mm.
4. Dimensions exclusive of mold gate burrs.
5. No mold flash allowed on the top and bottom lead surface.

	MILLIMETERS			INCHES		
Dim	Min	Nom	Max	Min	Nom	Max
A	1.00	–	1.10	0.039	–	0.043
b	0.25	0.30	0.35	0.010	0.012	0.014
c	0.1	0.15	0.20	0.004	0.006	0.008
c1	0	–	0.038	0	–	0.0015
D	2.95	3.05	3.10	0.116	0.120	0.122
E	1.825	1.90	1.975	0.072	0.075	0.078
E_1	1.55	1.65	1.70	0.061	0.065	0.067
e	0.65 BSC			0.0256 BSC		
L	0.28	–	0.42	0.011	–	0.017
S	0.55 BSC			0.022 BSC		
α	5°Nom			5°Nom		

RECOMMENDED MINIMUM PADS FOR DFN3x2



Recommended Minimum Pads
Dimensions in Inches/(mm)

Disclaimer

All products due to improve reliability, function or design or for other reasons, product specifications and data are subject to change without notice.

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Material Category Policy

Taiwan VBsemi Electronics Co., Ltd., hereby certify that all of the products are determined to be oHS compliant and meets the definition of restrictions under Directive of the European Parliament 2011/65 / EU, 2011 Nian. 6. 8 Ri Yue restrict the use of certain hazardous substances in electrical and electronic equipment (EEE) - modification, unless otherwise specified as inconsistent.(www.VBsemi.com)

Please note that some documents may still refer to Taiwan VBsemi RoHS Directive 2002/95 / EC. We confirm that all products identified as consistent with the Directive 2002/95 / EC European Directive 2011/65 /.

Taiwan VBsemi Electronics Co., Ltd. hereby certify that all of its products comply identified as halogen-free halogen-free standards required by the JEDEC JS709A. Please note that some Taiwanese VBsemi documents still refer to the definition of IEC 61249-2-21, and we are sure that all products conform to confirm compliance with IEC 61249-2-21 standard level JS709A.